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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Applicant: Sameh S. Rezeq, et al. Docket Number: TI-36599

Serial No.: 10/821,487 Art Unit: 2819

Filed: 04/09/04 Examiner: Howard L. Williams

For: High-Speed MASH Sigma-Delta Modulator Architecture and Method of Operation Thereof

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___ CONTINUATION APP'N	
___ DIVISIONAL APP'N	

NAME OF INVENTOR(S): Sameh S. Rezeq, et al.	RECEIPT DATE & SERIAL NO.: Serial No.: 10/821,487 Filing Date: 04/09/04
TITLE OF INVENTION: High-Speed MASH Sigma-Delta Modulator Architecture and Method of Operation Thereof	
TI FILE NO.: TI-36599 / DEPOSIT ACCT. NO.: 20-0668	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sameh S. Rezeq, et al. **Art Unit: 2819**

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For: HIGH-SPEED MASH SIGMA-DELTA MODULATOR ARCHITECTURE AND METHOD OF OPERATION THEREOF

Commissioner of Patents
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Karen Vertz 2-17-06
Karen Vertz Date

Transmitted herewith is an Appeal Brief in the above-identified application. The Commissioner is hereby authorized to charge the ***$500.00*** fee for this appeal, or credit any overpayment to Account No. 20-0668.

Respectfully submitted,

Alan K. Stewart
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APPELLANTS' BRIEF UNDER 37 C.F.R. §1.192

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Karen Vertz 2-17-06
Karen Vertz Date

Dear Commissioner:

The following Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed September 20, 2005. Please charge all required fees, including any extension of time fees, to the deposit account of Texas Instruments Incorporated, Deposit Account No. 20-0668.

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REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

Claims 1-28 are the subject of this appeal. Claims 1-28 are rejected. This application was filed on April 9, 2004.

STATUS OF THE AMENDMENTS

The Appellants filed an amendment under 37 C.F.R. § 1.111 on August 11, 2005 in response to the Office Action dated May 12, 2005. The Appellants filed an amendment under 37 C.F.R. § 1.116 on November 18, 2005 in response to the Office Action dated September 20, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

Specification page 8, line 1 to page 12, line 11, provides a concise explanation of the invention defined in independent claim 1. The present invention is founded on the broad recognition that narrower accumulators operate faster than wider accumulators and therefore that a sigma-delta modulator can be made faster by splitting the accumulators into multiple parallel chains of narrower accumulators and dividing the various bits of the input number between or among the chains. Any delays necessary to align the output bits are straightforward relative to schemes that require the entire sigma-delta modulator to be partitioned.

Referring initially to FIGURE 1, illustrated is a schematic diagram of one embodiment of a MASH3 sigma-delta modulator, generally designated 100, constructed according to the principles of the present invention. The MASH3 sigma-delta modulator 100 includes a splitter 110, a lower-order accumulator chain 120, a higher-order accumulator chain 130, pre-accumulator delay logic 160, inter-accumulator delay logic 170 and a combiner 180.

The MASH3 sigma-delta modulator 100 is configured to receive 12 parallel bits of an input number. Typically, the input number is generated from data input of a digital-to-analog converter. The MASH3 sigma-delta modulator 100 operates like a conventional MASH3 sigma-delta modulator, except instead of processing the entire input number in a single accumulator chain, the MASH3 sigma-delta modulator 100 divides the input number and employs the lower-order accumulator chain 120 and higher-order accumulator chain 130 to process half of the 12 input number bits apiece.

The splitter 110 is a conventional splitter coupled to the lower-order accumulator

chain 120 and the higher-order accumulator chain 130. The splitter 110 is configured to receive and then divide the 12 bit input number into six higher-order bits and six lower-order bits. Thus, the lower-order bits equal in number to the higher-order bits. Of course, in other embodiments, the number or high order bits may differ from the number of low-order bits. The six lower-order bits are sent to the lower-order accumulator chain 120 and the six higher-order bits are sent to the higher-order accumulator chain 130.

The lower-order accumulator chain 120 employs three six bit accumulators coupled together in series to process the six lower-order bits of the input number. The higher-order accumulator chain 130 also employs three six bit accumulators coupled together in series to process the six higher-order bits of the input number. The MASH3 sigma-delta modulator 100 therefore has an equal number of accumulators in the lower-order accumulator chain 120 and the higher-order accumulator chain 130. The number of accumulators in each accumulator chain 120, 130 is equal to the given order of the MASH3 sigma-delta modulator 100: three. Thus, the lower-order accumulator chain 120 and the higher-order accumulator chain 130 provide three stages of bit processing for the lower-order bits and the higher-order bits, respectively. In one embodiment, the lower-order accumulator chain 120 and the higher-order accumulator chain 130 are embodied in a deep-submicron complementary metal-oxide semiconductor integrated circuit. The six bit accumulators of both the lower-order accumulator chain 120 and the higher-order accumulator chain 130 are conventional accumulators well known by one skilled in the art.

Associated with the higher-order accumulator chain 130 is the pre-accumulator delay logic 160. The pre-accumulator delay logic 160 receives the high-order bits from the splitter 110 and provides a delay therefore before processing by the first accumulator of the higher-order accumulator chain 130. Also associated with the higher-order accumulator chain 130, and additionally the lower-order accumulator chain

120, is the inter-accumulator delay logic 170. The inter-accumulator delay logic 170 provides appropriate delays during processing of the high-order and the low-order bits to ensure alignment of bits. Since there is only one accumulator chain in a conventional MASH3 sigma-delta accumulator, the pre-accumulator delay logic 160 and the inter-accumulator delay logic 170 are not required to ensure proper alignment of bits during processing. The pre-accumulator delay logic 160 and the inter-accumulator delay logic 170 may include conventional digital delays typically employed to delay bits of data.

The combiner 180 is coupled to both the lower-order accumulator chain 120 and the higher-order accumulator chain 130 and is configured to align results therefrom to generate output bits of a given order. The combiner 180 may be a conventional combiner employed in common MASH3 sigma-delta modulators. The combiner 180 can provide an output in a unit-weighted format. Thus, a final arithmetic operation to obtain a digital binary or analog proportional signal can be deferred to subsequent operations performed by a digital-to-continuous domain converter coupled thereto.

Carryouts of each accumulator of the lower-order accumulator chain 120 are coupled to an accumulator of a corresponding stage of the higher-order accumulator chain 130. The carryouts of each accumulator of the higher-order accumulator chain 130 are coupled to the inter-accumulator delay logic 170 or the combiner 180. This differs from a conventional MASH3 sigma-delta modulator where all of the carryouts of the single accumulator chain are coupled to the combiner 180.

A clock signal (CLK in FIGURE 1) is provided to the MASH3 sigma-delta modulator 100 for a synchronous operation. The MASH3 sigma-delta modulator 100 performs a 12 bit addition by the first accumulator of the lower-order accumulator chain 120 adding the six lower-order bits in a first clock cycle while the six higher-order bits are delayed by the pre-accumulator delay logic 160. In a next clock cycle, the first accumulator of the higher-order accumulator chain 130 adds the six higher-order bits

with the carryout from the first accumulator of the lower-order accumulator chain 120. Subsequent 12 bit additions are similarly performed by the second and third stage accumulators of the lower-order accumulator chain 120 and the higher-order accumulator chain 130 with the inter-accumulator delay logic 170 providing the proper delays between clock cycles to ensure proper alignment.

A reset signal (arstz) is also provided for each stage of the MASH3 sigma-delta modulator 100. The reset signals allow stage reductions of the sigma-delta modulator 100 by powering-down stages thereof. For example, instead of a third order modulator, arstz3 may be asserted to reset the third stage of the sigma-delta modulator 100 and provide a second order modulator. For a third order modulator, arstz1, arstz2 and arstz3 will not be asserted such that each stage is not reset (unreset). Operation of the reset signals may be controlled by user input.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-28 stand rejected under 35 U.S.C. § 102 (b) as being anticipated by U.S. Patent No. 5,079,551.

ARGUMENT

Rejection under 35 U.S.C. § 102 (b) over U.S. Patent No. 5,079,551

Claims 1-28

Claim 1 includes a lower-order accumulator chain for processing only lower order bits and a higher-order accumulator chain for processing only higher-order bits. The references of record do not show, teach, or suggest these limitations. The Kimura reference does not show, teach, or suggest the accumulator chains of Claim 1. U.S. Patent No. 5,079,551 discloses an addition circuit for adding feedback digital data to input data. U.S. Patent No. 5,079,551 does not show accumulator chains.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-28 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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CLAIMS APPENDIX

1. A sigma-delta modulator, comprising:

a lower-order accumulator chain configured to process only lower-order bits of an input number;

a higher-order accumulator chain configured to process only higher-order bits of said input number; and

a combiner coupled to both said lower-order and higher-order accumulator chains and configured to align results therefrom to generate output bits of a given order.

2. The sigma-delta modulator as recited in Claim 1 wherein said lower-order bits equal in number said higher-order bits.

3. The sigma-delta modulator as recited in Claim 1 wherein accumulators in said lower-order accumulator chain equal in number both accumulators in said higher-order accumulator chain and said given order.

4. The sigma-delta modulator as recited in Claim 1 wherein said higher-order accumulator chain has pre-accumulator delay logic associated therewith.

5. The sigma-delta modulator as recited in Claim 1 wherein said lower-order accumulator chain and said higher-order accumulator chain have inter-accumulator delay logic associated therewith.

6. The sigma-delta modulator as recited in Claim 1 further comprising at least one other accumulator chain.

7. The sigma-delta modulator as recited in Claim 1 wherein said lower-order accumulator chain and said higher-order accumulator chain are embodied in a deep-submicron complementary metal-oxide semiconductor integrated circuit.

8. The sigma-delta modulator as recited in Claim 1 wherein said lower-order accumulator chain and said higher-order accumulator chain have multiple stages and each of said multiple stages is controlled by an unique reset signal.

9. A method of performing sigma-delta modulation, comprising:

processing only lower-order bits of an input number in a lower-order accumulator chain;

processing only higher-order bits of said input number in a higher-order accumulator chain; and

aligning results from both said lower-order and higher-order accumulator chains to generate output bits of a given order.

10. The method as recited in Claim 9 wherein said lower-order bits equal in number said higher-order bits.

11. The method as recited in Claim 9 wherein accumulators in said lower-order accumulator chain equal in number both accumulators in said higher-order accumulator chain and said given order.

12. The method as recited in Claim 9 wherein said higher-order accumulator chain has pre-accumulator delay logic associated therewith.

13. The method as recited in Claim 9 wherein said lower-order accumulator chain and said higher-order accumulator chain have inter-accumulator delay logic associated therewith.

14. The method as recited in Claim 9 further comprising processing other bits of said input number in at least one other accumulator chain.

15. The method as recited in Claim 9 wherein said lower-order accumulator chain and said higher-order accumulator chain are embodied in a deep-submicron complementary metal-oxide semiconductor integrated circuit.

16. The method as recited in Claim 9 wherein said lower-order accumulator chain and said higher-order accumulator chain have multiple stages and said method further comprises controlling each of said multiple stages by an unique reset signal.

17. An digital-to-analog converter, comprising:

digital circuitry configured to provide input numbers from a digital input;

a sigma-delta modulator coupled to said digital circuitry and including:

a lower-order accumulator chain that processes only lower-order bits of said input numbers,

a higher-order accumulator chain that processes only higher-order bits of said input numbers, and

a combiner, coupled to both said lower-order and higher-order accumulator chains, that aligns results therefrom to generate output bits of a given order; and

a digital-to-continuous converter, coupled to said sigma-delta modulator, that converts said output bits into a continuous domain.

18. The digital-to-analog converter as recited in Claim 17 wherein said sigma-delta modulator is a multistage noise shaping (MASH) sigma-delta modulator.

19. The digital-to-analog converter as recited in Claim 17 wherein said input digital circuitry includes an upsampler or an interpolator.

20. The digital-to-analog converter as recited in Claim 17 wherein said lower-order bits equal in number said higher-order bits.

21. The digital-to-analog converter as recited in Claim 17 wherein accumulators in said lower-order accumulator chain equal in number both accumulators in said higher-order accumulator chain and said given order.

22. The digital-to-analog converter as recited in Claim 17 wherein said higher-order accumulator chain has pre-accumulator delay logic associated therewith.

23. The digital-to-analog converter as recited in Claim 18 wherein said lower-order accumulator chain and said higher-order accumulator chain have inter-accumulator delay logic associated therewith.

24. The digital-to-analog converter as recited in Claim 17 further comprising at least one other accumulator chain.

25. The digital-to-analog converter as recited in Claim 17 wherein said lower-order accumulator chain and said higher-order accumulator chain are embodied in a deep-submicron complementary metal-oxide semiconductor integrated circuit.

26. The digital-to-analog converter as recited in Claim 17 wherein said lower-order accumulator chain and said higher-order accumulator chain have multiple stages and each of said multiple stages is controlled by an unique reset signal.

27. The digital-to-analog converter as recited in Claim 17 wherein said digital-to-continuous converter includes a digitally-controlled RF power amplifier and said digital-to-analog converter is a digital-to-RF amplitude converter.

28. The digital-to-analog converter as recited in Claim 17 wherein said generated output bits are in a unit-weighted format and said digital-to-continuous converter employs a unit-weighted element for processing thereof.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.